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Power Quality Improvement of Three Phase Four Wire System using Modified UPQC Topology

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Abstract: **Unified Power Quality Conditioner is a versatile custom power device which mitigates voltage and current related Power Quality issues in distribution system. Modified UPQC topology dealt in this which uses a common DC link voltage for both series and shunt active filter, thus overcoming the need for capacitor voltage balancing in conventional UPQC topology. In this topology, interfacing inductor of shunt active filter is connected in series with a capacitor. The fourth leg of the VSI is connected to negative terminal of DC link and thus eliminates the requirement of fourth leg of VSI. Switching signals are generated using hysteresis band current controller and Icos ϕ algorithm for the operation of UPQC. The performance of modified UPQC topology with hysteresis band current controller and Icosϕ algorithm has been analyzed and comparison has been done using Matlab/simulink.**

1. INTRODUCTION

Present days, power quality problems are the major concerns for the consumers and to the industrial sectors. Power quality problems are mainly because of the power semiconductor devices and the electronic controllers which are used in industries are very sensitive to voltage quality. With the poor voltage quality, harmonics of the system increases and leads to the poor power quality. The different power quality mitigation techniques like SVC, STATCOM, TCSC and UPQC comes under the FACTS controllers mainly designed for enhancing the power quality improvement and reliability.

Devices like DVR, DSTATCOM and UPQC etc are mainly used for improving power quality of voltage and current [1]. Among all the devices UPQC gives the best results for the power quality. This is the combination of both the series and shunt active filters. Series active filter (DVR) is connected to source side, mainly reduces the load voltage harmonics and eliminates the supply voltage imbalances. Shunt active filter (DSTATCOM) which is connected to the load side, reduces the source current harmonics and compensates the load reactive power [2]. Configuration of UPQC needs two inverters side by side. UPQC solves the source current and load voltage imperfections. The structure of UPQC shown in Fig.1

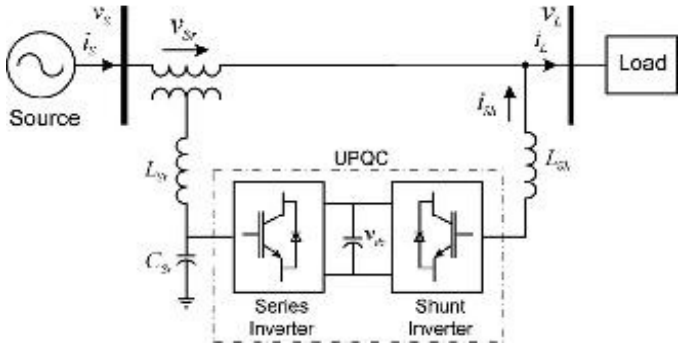


Figure 1. Structure of UPQC

The performance of active filter is influenced by the dc-link capacitor voltage values. For the shunt active filter, dc link capacitor voltage rating must be greater than the line to neutral voltage. For distortion free compensation, the dc link voltage required must be higher or equal to 1.6 times the phase voltage. Similarly for a better series compensation of voltages, the series active filters dc link voltage maintained at a value to the peak of line to line voltage [3]. In the case of UPQC, the capacitor value is not same for both the shunt and series filters. There is a mismatch happening in the dc capacitor voltage requirement for the filters. So, in order to avoid this mismatching, it is proposed [7] to use a common dc link capacitor ratings which satisfy the dc link voltage requirement for both the filters.

For general 3phase 4wire systems, neutral clamped topology [4,5] is used which requires the independent control for both series and shunt inverters, but problem in this case is it requires capacitor voltage balancing. In this paper the modified topology [7], capacitor is connected in series with the shunt filter inductor, reduces the dc link capacitor voltage for shunt active filter and compensates the reactive power to the load. By the addition of capacitor, it allows the matching of the dc link voltage requirement for both series and shunt active filters with a common dc link capacitor. To avoid the

necessity of fourth leg in VSI of the shunt active filter, the system neutral is connected to negative side of dc bus.

The controller plays an important role in the performance of UPQC. Some of the control strategies mentioned in literature [6] which were used for UPQC are P-q-r theory, modified p-q theory, synchronous reference frame theory, Unit vector template technique etc. In this paper, UPQC is mainly tested for the power quality improvement by a) Reducing the THD's of source currents and load voltages b) power factor correction and d) Mitigation of Voltage sags. This has been simulated and analyzed with hysteresis band current controller and Icos ϕ algorithms, the comparison of both algorithms has been explained in detail in section IV.

2. MODIFIED UPQC TOPOLOGY

The modified topology of UPQC [7] is explained in detail. Fig 2 shows the power circuit of the VSI topology for UPQC compensated system. In this figure, the source voltages of phases a, b, and c are termed as V_{sa}, V_{sb}, and V_{sc} respectively. The source terminal voltages are V_{ta}, V_{tb} and V_{tc}. The injected voltages of the series active filter are V_{dvra}, V_{dvrb}, and V_{dvrc} respectively. The three phase source currents are represented as i_{sa}, i_{sb} and i_{sc} and the load currents are i_{la}, i_{lb} and i_{lc}. The shunt active filter currents are denoted as i_{fa}, i_{fb} and i_{fc}. L_s and R_s are the source inductance and impedance. L_f and R_f are the filter parameters of the shunt active filter. L_{se} and R_{se} are filter parameters of the series active filter respectively. The load used here is shown as unbalanced linear load and non linear loads

Modified UPQC topology has single capacitor in DC link when compared to conventional UPQC which has two DC storage devices in DC link. In conventional UPQC topology series and shunt inverters are controlled independently. Modified UPQC topology are more preferred that conventional because of reduced DC storage device even though it has advantages like smooth tracking with less number of switches. In the modified topology, neutral wire has been connected to negative edge of dc bus, in addition to that capacitor C_f is connected in series with the inductor of the shunt active filter. The capacitor connected in series, supplies the part of reactive power required by the load and active filter will compensates the balance reactive power and the harmonics present in the load. This topology avoids the over ratings of the series active filter of the UPQC compensation system and also avoids the need of balancing the dc link voltages [7].

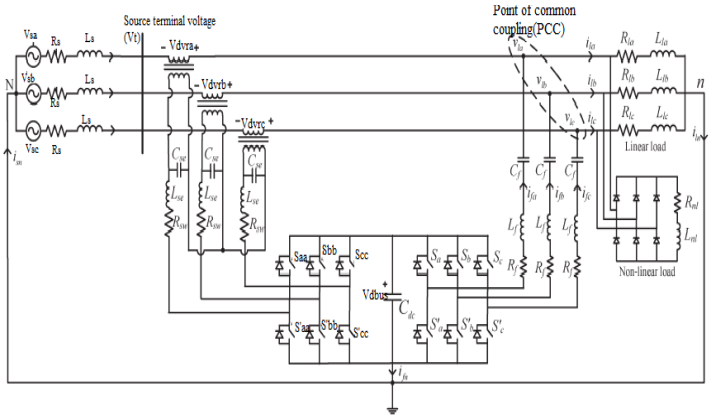


Figure 2.Power circuit of VSI topology for UPQC compensated system

3. CONTROLLER STRATAGIES OF UPQC

The main aim of the controller strategies is to generate the reference signals for the APF's of UPQC. The distortions of the load current and source voltage are extracted using the control technique. The elimination of voltage harmonics at the source side is carried out by controlling the series active filter. Similarly, for the alleviation of the source currents from the harmonics, balancing the currents and the reactive power compensation mainly done by controlling the shunt active filter. The control strategies for the operation of UPQC are explained in detail.

A. Hysteresis band current controller

The terminal voltage has been distorted due to the flow of distorted load current through feeder impedance. Voltage at PCC can be made sinusoidal and balanced using series active filter. However voltage continues to distort. Since the terminal voltage is distorted, current reference for shunt filter cannot be generated. This limitation can be overcome by extracting fundamental positive voltage sequences $V_{la}^{+}, V_{lb}^{+}, V_{lc}^{+}$ at PCC. The equations for reference compensator currents are given below. The DC capacitor voltage PI controller generates the P_{loss} term which is the combination of both switching and ohmic losses in actual compensator. The reference filter currents are given below[7].

$$i_{fa}^{*} = i_{la} - i_{sa}^{*} = i_{la} - \frac{v_{la1}^{+} + \gamma(v_{lb1}^{+} - v_{lc1}^{+})}{\Delta_1^{+}}(P_{lavg} + P_{loss})$$

$$i_{fb}^{*} = i_{lb} - i_{sb}^{*} = i_{lb} - \frac{v_{lb1}^{+} + \gamma(v_{lc1}^{+} - v_{la1}^{+})}{\Delta_1^{+}}(P_{lavg} + P_{loss})$$

$$i_{fc}^{*} = i_{lc} - i_{sc}^{*} = i_{lc} - \frac{v_{lc1}^{+} + \gamma(v_{la1}^{+} - v_{lb1}^{+})}{\Delta_1^{+}}(P_{lavg} + P_{loss}) \quad \text{……..} \quad (1)$$

where

$$\Delta = \sum_{j=a,b,c} (v_{lj1}^{+})^2$$

j= a,b,c γ=tan(ɵ/√3)

The phase angle between source voltage and currents is given as ɵ. Irrespective of distorted supply, the above algorithm gives compensated and balanced source currents. For series active filter, the reference voltages are generated as given in equation 2.

$$v_{dvri}^{*} = v_{li}^{*} - v_{ti} \quad (2)$$

i =a, b, c

v_{dvri}^{*} - Reference series filter voltages, v_{ti} - source terminal voltages, v_{li}^{*} - desired load voltages.

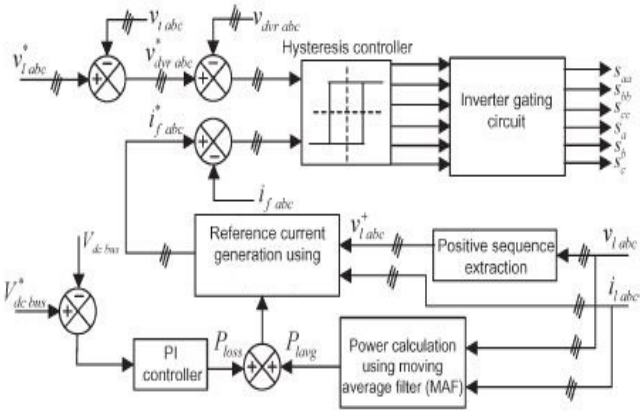


Figure 3. Block diagram of controller UPQC [7]

The controller block diagram is shown in Fig.3.The sensed actual and reference values calculated from the measurements. Switching pulses are generated by Hysteresis band current controller [7] is a two level comparator, based on feedback loop which generates the switching commands for the VSI switches and these switching commands are generated, whenever error value increases to particular tolerance band limit. For the shunt active filter, the switching done as follows

If $i_{fa} \geq i_{fa}^{*} + h_1$, then bottom switch is turned ON whereas top switch is turned OFF ($S_a = 0, S_a^{'} = 1$)

If $i_{fa} \leq i_{fa}^{*} - h_1$, then top switch is turned ON whereas bottom switch is turned OFF ($S_a = 1, S_a^{'} = 0$)

For the Series active filter, switching done as follows

If $V_{dvra} \geq V_{dvra}^{*} + h_2$, then bottom switch is turned ON whereas top switch is turned OFF ($S_{aa} = 0, S_{aa}^{'} = 1$)

If $V_{dvra} \leq V_{dvra}^{*} - h_2$, then top switch is turned ON whereas bottom switch is turned OFF ($S_{aa} = 1, S_{aa}^{'} = 0$).

From the controller, six pulses are generated and complimentary signals are used to controlling the 12 switches of two converters.

B. Icos ϕ algorithm

a) Reference voltage generation for series active filter:

The series active filter control algorithm [8] is given in Fig 4. To synchronize with the supply voltages, a PLL (Phase Locked Loop) is used for the distorted source voltages. The distorted source voltages are given to PLL and it evaluates the 2 quadrature unit matrices (i.e. $\sin \omega t$ & $\cos \omega t$). The output of PLL (i.e sine and cosine) are used to calculate all the three phases with a displacement of 120^0, three unit vectors are given below in equation (3)

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin \theta \\ \cos \theta \end{bmatrix} \quad (3)$$

where u_a , u_b and u_c are the three unit vectors

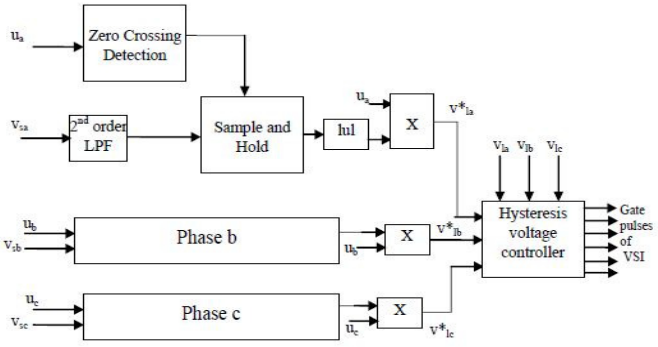


Figure 4.. Series active filter controller

The extraction of amplitude of fundamental source voltage is done at the zero crossing of the unit template of the source voltages which are in phase with each other. This procedure involves the shifting of source voltage by +90° using a set of low pass filters. In order to obtain the magnitude of source voltage, the cutoff frequency of the low pass filter is maintained at 50Hz.The determination of amplitude of in phase sine waveforms is done by using the zero crossing detector and sample and hold circuits. Finally, reference load voltages $(V_{la}^{*}, V_{lb}^{*}, V_{lc}^{*})$ are obtained as the product of

fundamental supply voltages and to the unit vectors as given below.

$$[V_{la}^{*}] = [V_{sa1}].[u_a];$$
$$[V_{lb}^{*}] = [V_{sb1}].[u_b];$$
$$[V_{lc}^{*}] = [V_{sc1}].[u_c] \quad (4)$$

where V_{sa1} , V_{sb1} and V_{sc1} are magnitudes of fundamental source voltages of phase a, b and c respectively. The reference load voltages are compared with the actual load voltages and then given to hysteresis controller and switching signals are generated. Generated switching signal are given to the six switches of Series Active Filter.

b) Reference current generation of shunt APF

The controller for shunt active filter [9-10] mainly for the generation of reference currents (i.e $i_{sa}^{*}, i_{sb}^{*} i_{sc}^{*}$) to eliminate the current harmonics and balancing the source currents. The shunt active filter control algorithm is given in Fig 5.For the shunt active filter, the fundamental load current component of current is extracted at the zero crossing of the source voltages which are in phase with each other. The source voltages are shifted by 90 degrees using a set of low pass filters. The cut off frequency of these low pass filter is maintained at 50Hz. The sample and hold circuits and zero cross detectors are used to extract the Icos ϕ component from the load current at PCC. The obtained reference source currents are compared with the actual source currents and then given to hysteresis controller and switching signals are generated. Generated switching signal are given to the six switches of Shunt Active Filter.

The block diagram of shunt active filter controller is given below:

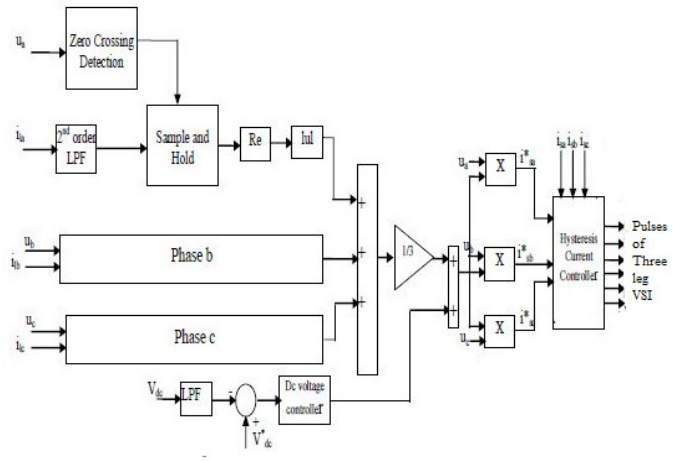


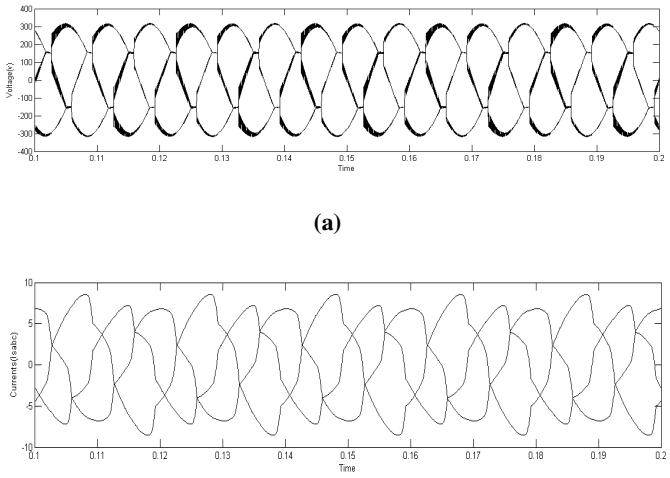
Figure5. Shunt active filter controller

4. SIMULATION RESULTS

The UPQC topology is developed by using MATLAB/simulink platform. The simulated results of the UPQC topology by using both the controllers (1.Hysteresis band current controller and 2.Icos ϕ algorithm) are given in this section. For good understanding, the results are tabulated and comparison has been done. The simulation model of UPQC (shown in Fig.7) consists of three single phase sources connected in star with a phase shift of 120 degrees apart with a neutral wire with voltages of 400V (line to line), frequency (50Hz) and having the load of both linear as well as non linear loads. The system feeder impedance is taken as Z_s =1+j3.141Ω. Three linear transformers of 1:1, 1000VA and 230V are connected in series with all the three phases and a capacitor (80μF) is connected across the secondary of the transformers shown in fig 7. For harmonics in the source voltages, a three phase diode rectifier is used. The load is a combination of both the unbalanced linear loads (a) Z_{la}=34+j47.5 Ω, b) Z_{lb}=81+j39.6 Ω, c) Z_{lc}=31.5+j70.9 Ω) and diode bridge rectifier with R=150Ω and L=300mH as non linear loads.

The load parameters and the circuit parameters are presented in the Appendix.

The simulation results of the three phases four wire system without compensation is obtained as shown in Fig 6. Before compensation, the source currents and load voltages are distorted and unbalanced as shown in Fig 6.



(a)

Figure 6. Load voltages and source currents before compensation

A. Simulation model of UPQC with hysteresis band current controller

The simulation model of UPQC with hysteresis band controller is shown in Fig.7

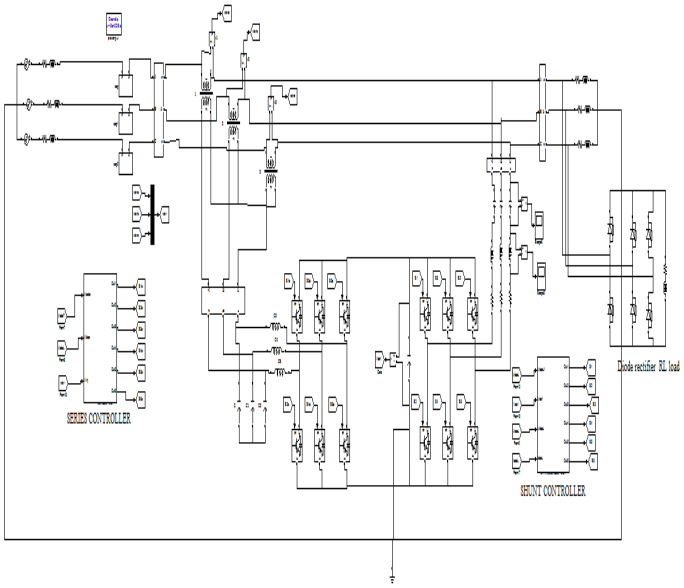
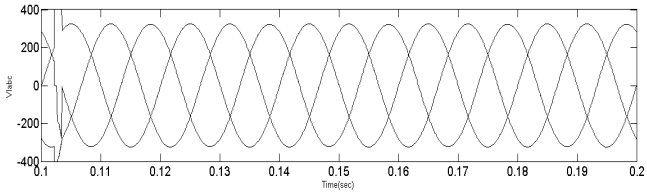
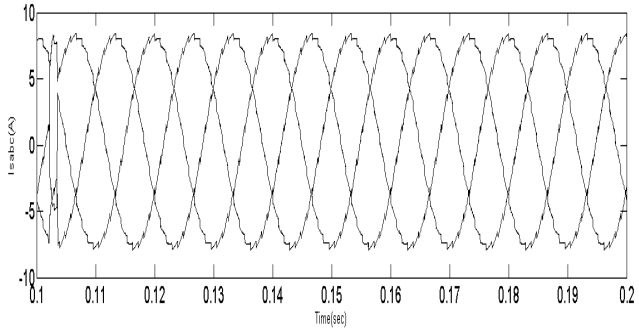


Figure 7. Matlab simulation model of UPQC topology

The main purpose of the UPQC is to reduce the imperfections in both voltages and currents and makes them as harmonics less (reduces the THD values). After connecting the UPQC the load voltages are balanced and become distortion free shown in Fig 8(a) and the source currents are also balanced and distortion free as shown in Fig.8(b)



(a)



(b)

Figure 8. a) Load voltages and b) Source currents after compensation

Power factor of the system is obtained as 0.95 as shown in Fig.8(c)

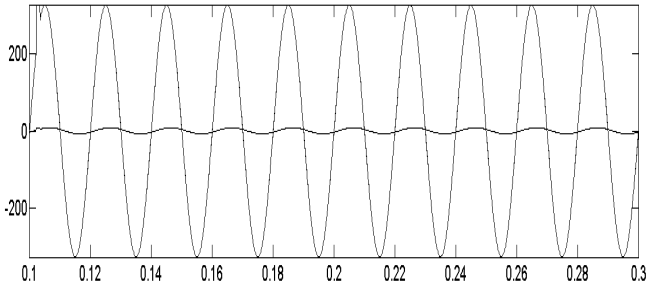


Figure 8.c) Power Factor

The load voltages and source currents after compensation are shown in Fig 8(a) and Fig 8(b).The THD's load voltages and the source currents of the system without UPQC is found as 9.80 %, 8.98 % and 8.08 % respectively and the source current THD's are 10.74%, 12.10% and 13.14% respectively. This THD level gives low quality supply. While controlling the system in closed loop by UPQC the THD level found to be reduced as 2.61 %, 2.65% and 2.86 % respectively for source currents and the load voltage THD values are 0.95%, 0.91 % and 1% respectively. Overall system losses can be reduced by controlling the THD level. The power factor of the system is obtained as 0.95 which is good to the system as shown in figure Fig.8(c).

B. Simulation model of UPQC using Icos ϕ algorithm

The same circuit of UPQC is simulated with Icos ϕ algorithm. The simulation model with Icos ϕ controller is shown in Fig.9. The parameters used are same as given in the appendix but for getting proper results filter parameters are tuned.

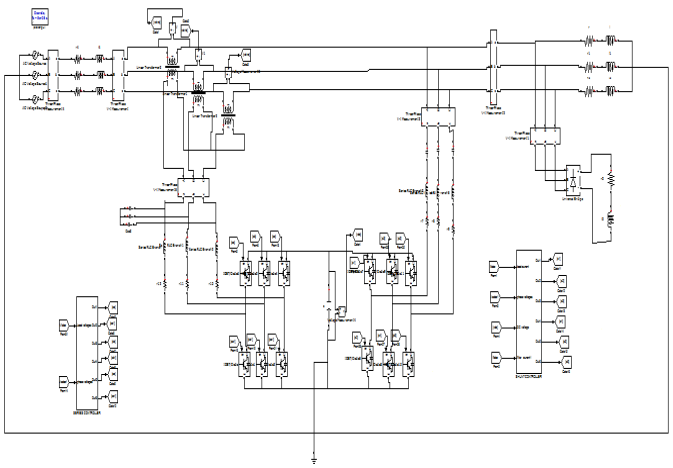
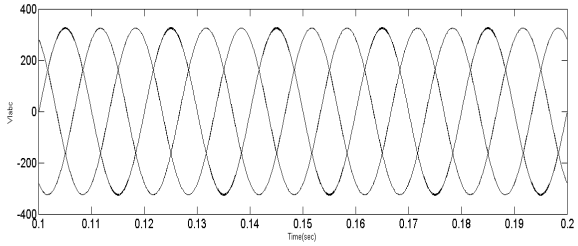
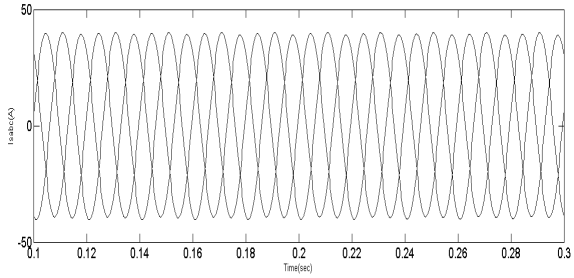


Figure 9.Simulation model of UPQC with Icosϕ algorithm

The Load voltages and source currents of the circuit after compensation are shown in Fig.10. Load voltages are balanced and become harmonic less and source currents are also become balanced and harmonic less.



(a)



(b)

Figure 10.a) Load voltage and b) source currents after compensation

Power factor calculation of the system obtained as 0.98 which is better as compared to the Hysteresis controller as shown in Fig.11.

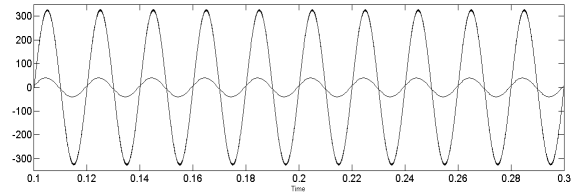
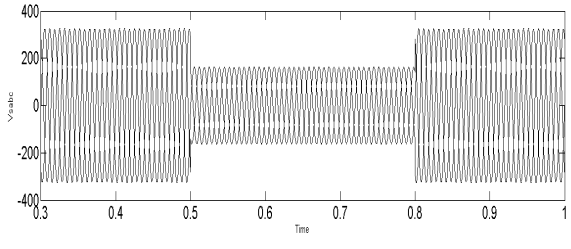
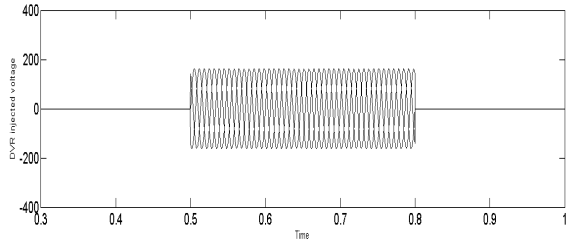


Figure 11. Power factor =0.98

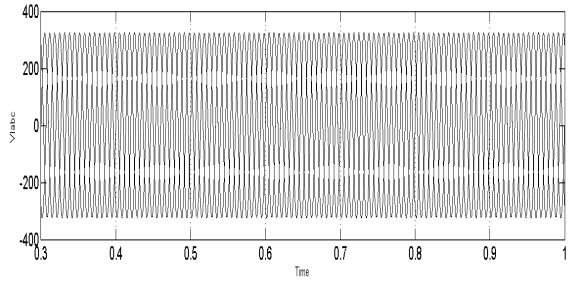
For the controlling of UPQC, Icos ϕ algorithm has been used and the THD values are reduced. Before compensation THD values of the system for load voltages THD's are found as 9.80 %, 8.98 % and 8.08 % respectively and the source current THD's are 10.74%, 12.10% and 13.14% respectively. The values of the THD after compensation are obtained for load voltages are 1.96%, 1.74% and 1.79% respectively and for source currents found as 2.99%, 2.97 % and 2.99% respectively. The series active filter mitigates the sag problems and maintains the desired load voltages. In all the three phases, the 50% of sag is taken and starts at 0.5s and ends at 0.8s. The performance of the series compensator is given in Fig.12.The source voltages with sag are shown in Fig.12 (a), DVR injected voltages in Fig.12 (b) and the desired load voltages in Fig.12(c).



(a)



(b)



(c)

Figure 12. Series compensator performance a) source terminal voltages b) DVR injected voltages and c) load voltages

5. PERFORMANCE COMPARISON OF CONTROLLERS

For the operation of UPQC, both the controllers (Hysteresis band current controller and $I\cos\Phi$ algorithm) showing the better results. By using both the controllers the THD values obtained are less than 5% according to IEEE standard. For both the controllers, there is a slight difference of 0.4% in the THD values for source currents and for Load voltages 0.9%. Power factor calculations of the system using both the controllers are 0.95(for Hysteresis controller) and 0.98(for $\text{Icos}\Phi$ algorithm).THD values of both the controllers are tabulated and given below:

Table I.: % THD values of the supply currents and load voltages

Supply currents/ load voltages	Without UPQC	With UPQC (Hysteresis band current controller)	With UPQC (Icosϕ algorithm)
Isa	10.74 %	2.61 %	2.99 %
Isb	12.10 %	2.65 %	2.97 %
Isc	13.14 %	2.86 %	2.99 %
Vla	9.80 %	0.95 %	1.96 %
Vlb	8.98 %	0.91 %	1.74 %
Vlc	8.08 %	1.0 %	1.79 %

6. CONCLUSION

The three phase four wire UPQC is simulated with both the controllers (Hysteresis band current controller and $I\cos\Phi$ algorithm) and the results are compared with the simulation results using Matlab/Simulink. Based on various power quality improvements such as load balancing, power factor correction, elimination voltage and current harmonics and mitigation of voltage sags, the performance of UPQC is satisfactory. Both the controllers show better performances with a slight difference in THD values. The THD values are reduced to less than 5% which is IEEE standard. Performance of UPQC with both the controllers are tabulated with the obtained %THD values and given in table no.1.

APPENDIX

Supply voltage: 230V (line to ground), 50Hz

R_s = 1Ω, L_s =10mH

Series filter parameters: L_{se} =5mH, C_{se} =80μF

Shunt filter parameters: L_{sh} =26mH, C_{sh} =65μF,

R_{sh} =0.1Ω

DC link capacitance: C_{dc} = 3300μF

Transformer: 1KVA, 230V, 1:1

K_p =0.5, K_i =2

Loads: 1) Unbalanced linear loads a) Z_{la} =34+j47.5 Ω, b) Z_{lb} =81+j39.6 Ω, c) Z_{lc} =31.5+j70.9 Ω

2) Non linear load as diode bridge rectifier with $R = 150\Omega$ and $L = 300mH$ load.

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